Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC3024 Low Power VLSI Design

Set A

Time : 3 hrs
Total Marks: 100

1. a).A 32 bit off-chip bus operating at 3.3V and 400 MHz clock rate is driving a capacitance of 25pF/ bit. Each bit is estimated to have a toggling probability of 0.5 at each clock cycle. What is the power dissipation in operating the bus? (5)

   b).Derive an expression for dynamic power dissipation in a CMOS inverter due to charging and discharging of capacitance. (9)

   c).Explain about architectural level power analysis. (6)

OR

2. a). The chip size of a CPU is 25mm x 40 mm with clock frequency of 600MHz operating at 2.0 V. The length of the clock rouing is estimated to be twice the circumference of the chip. Assume that the clock frequency is routed on a metal layer with width of 1.5µm and the parasitic capacitance of the metal layer is 2Ff/µm^2. What is the power dissipation of the clock signal? (5)

   b). Discuss the variation of short circuit current of a CMOS inverter for input signal slope and output load capacitance.10)

   c) Derive an expression which relates static probability and frequency. (5)

3. a). Explain in detail about the power and delay of an inverter chain using transistor sizing. (8)

   b).Explain in detail about Equivalent Pin Ordering and Network Restructuring and Reorganization. (12)

OR

4. a).Explain with neat diagrams the single and double edge triggered FFs and compare their power consumption. (8)

   b) Explain the architecture of Bus invert encoding. Analyze its performance in terms of efficiency. (12)

5. a) Discuss in detail about the Precomputation Logic Technique with an example. (14)

   b).How to take precautions to avoid floating node in CMOS circuits to reduce power consumption. (6)

OR

6. a). Explain in detail various Power Reduction Techniques in Clock Networks. (14)

   b). Explain in detail the power management techniques to reduce power in architecture level (6)

7. a).Show how parallelism has been used to improve computation throughput of high performance digital systems. (10)

   b). Explain in detail the organization of a RAM and also explain the operation of 6T MOS static RAM memory cell. (10)

OR

8. a). Explain the deep sub micrometer device design issues and the key to minimize short channel effects. (6)

   b). Explain in detail the Low Voltage circuit design techniques. (14)

9. Compulsory:

a). Explain the concepts of energy recovery circuit design. (10)

b). Explain the methods of reducing power in Writer Driver circuits and Sense Amplifier circuits of SRAM core. (10)

Wishing you All the Best
